variable clock
external
memory.

Gate Array Functional Specification

Consumer Products Group
Calculator Division

8/31/81

Revision 0.6

SECTION 1

Introduction

1.1 Purpose of This Document

This document describes the operation and use of the gate array hardware. It is intended to be an aid to the development of product software and is not intended as an electrical specification of the gate array.

1.2 Organization of This Document

Each functional portion of the gate array is described separately. In addition, a quick reference chart is provided as the last section of this document. This document is organized in sections as follows:

Section 1 - Introduction

Section 2 - System Control Register

Section 3 - Address Control Register

Section 4 - I/O Bus Interface

Section 5 - Keyboard (Write) Latch

Section 6 - Power-on Hold Latch

Section 7 - Signal List

Section 8 - Quick Reference Chart

SECTION 2

System Control Register

2.1 General Information

The system control register is a 5 bit read/write latch which can be accessed at address >0119. Bit 0 is a Bus Control Enable (BCE) bit. Bits 1 and 2 are Page Control (PC1 & PC2) bits for the system ROM address area (>D000 - >EFFF). Bits 3 & 4 provide page control for use in the memory expansion address area. The function of each of these bits is further explained below.

System Control Register at address >0119

7	6	5	4	3	2	1	0
X	X	X	PC4	PC3	PC2	PC1	BCE

2.2 Bit 0 - Bus Control Enable (BCE)

The Bus Control Enable bit is a simple enable and operates according to the following chart.

BCE	FUNCTION
0	Inhibits control of bus available (BAV)
1	Allows control of bus available (BAV)

2.3 Bits 1 & 2 - System ROM Page Control (PC1,PC2)

These two paging bits allow for the use of up to 32K of system ROM arranged as four 8K pages and accessed in the 8K system ROM address space (>D000 - >EFFF). The function of these two bits will be as follows:

PC2	PC1	PAGE SELECTED
0	0	Lower 8K of 16K memory chip *Lowest 8K of 32K memory chip
0	1	Upper 8K of 16K memory chip *Second 8K of 32K memory chip
1	0	*Third 8K of 32K memory chip
1	1	*Highest 8K of 32K memory chip

*Allows for future availability of 32K ROM

If a 16K ROM is used, PC1 will be connected to the A13 address input line and PC2 will not be used. If a 32K ROM is used PC1 will be connected to A13 with PC2 connected to A14 of the address input lines of the ROM.

2.4 Bit 3 & 4 - Expansion Area Page Control (PC3,PC4)

These bits are intended for use in the expansion area (>5000 - >CFFF) to provide the capability of doubling either or both of the memory chips or increasing the size of one of the chips by a factor of four. This will allow a maximum capability of 80K bytes of memory in the expansion module. With the use of the Expansion Speed Control bits (ESC1,2) a variety of combinations of fast and slow memories are possible.

PC3	*Page Selected
0	Lower 16K of 32K memory chip
1	Upper 16K of 32K memory chip

*Based on future 32K ROM availability

PC3 would be connected to the A14 address input line of the 32K memory. If a 16K memory is used, PC3 will not be used.

SECTION 3

Address Control Register

3.1 General Information

The Address Control Register is a 6 bit read/write latch which can be accessed at address >0110. Bits 0 - 5 contain the control information and bits 6 - 7 are not used.

The following figure shows the bit assignments for the Address Control Register at address >0110

7	6	5	4	3	2	1	0
X	X	EAC2	EAC1	SRAC2	SRAC1	ESC2	ESC1

3.2 Address Control Scheme - Bits 2 - 3

The purpose of this address control fields (EAC, SRAC) is to allow for the use of two memory chips (each chip either 2K or 8K) in the system RAM (SRAC) address space while maintaining memory continuity within the address space. The address decoding scheme is shown in the following table:

System RAM Address Control (SRAC) - >1000 - >4FFF

SRAC2	SRAC1	MEMORY CONFIGURATION		ADDRESS SELECTION	
		Socket 1	Socket 2	Chip Enable Socket 1	Chip Enable Socket 2
0	0	8K	8K	1000-2FFF	3000-4FFF
0	1	8K	2K	1000-2FFF	3000-37FF
1	0	2K	8K	1000-17FF	1800-37FF
1	1	2K	2K	1000-17FF	1800-1FFF

Reverse?

3.3 Address Control Scheme - Bits 4 - 5

The purpose of this address control field (EAC) is to allow for flexibility in the selection of memory chips for the expansion address area (>5000 - >CFFF). The address decoding scheme is shown in the following table:

Expansion Area Address Control (EAC1,2) - >5000 - >CFFF

EAC2	EAC1	ADDRESS SELECTION	
		Chip Enable Socket 1(CE4)	Chip Enable Socket 2(CE5)
0	0	5000-57FF	5800-5FFF
0	1	5000-6FFF	7000-8FFF
1	0	5000-8FFF	9000-CFFF

3.4 Expansion Area Speed Control (ESC 1 & 2) - Bits 0 & 1

The purpose of these bits is to allow software to select whether the expansion area (>5000 - >CFFF) is actually treated as a fast or slow memory area. The function of these expansion speed control bits will be as follows:

CE4	ESC1	Clock
1	X	Normal
0	0	Normal
0	1	Stretched

CE5	ESC2	Clock
1	X	Normal
0	0	Normal
0	1	Stretched

SECTION 4

I/O Bus Interface

4.1 General Information

The gate array provides for 6 lines of the I/O bus. (Power and ground are provided elsewhere.) These 6 lines contain four data bits (D0-D3), a Bus Available line (BAV), and a Handshake line (HSK). These are accessed through three different addresses and are arranged as shown below:

I/O Bus Data Latch at address >0112

7	6	5	4	3	2	1	0
X	X	X	X	D3	D2	D1	D0

I/O Bus - Bus Available at address >0113

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	BAV

I/O Bus - Handshake at address >0114

7	6	5	4	3	2	1	0
LATD	X	X	X	X	X	LAT	HSK

4.2 I/O Bus Data Latch

The I/O data lines are addressed at >0112 and use a 4 bit, bi-directional, read/write latch. D0-D3 are connected, via the latch, to AD0-AD3 on the internal bus. On a write cycle the data is latched and the output 3-state buffers are enabled. The buffers remain enabled until the signal on the HSK line returns high (all active peripherals have acknowledged receipt). On a read cycle the input 3-state buffers are enabled and will pass the I/O bus data (D0-D3) to the main bus (AD0-AD3).

4.3 I/O Bus - Bus Available Latch

The Bus Available (BAV) line uses a 1 bit, bi-directional, read/write latch addressed at >0113. The output 3-state buffer is controlled by the Bus Control Enable (BCE) bit of the System Control Register described elsewhere in this document. When BCE is high the processor may control BAV. The state of the BAV latch is controlled by writing the desired state to the least significant bit of address >0113. The state of BAV may also be monitored by reading the least significant bit of the same address.

4.4 I/O Bus - Handshake Line

Handshake (HSK) is an open collector line which is controlled by a signal called LAT. HSK is high only when all units on the bus have released it. LAT may be set in two ways and reset in two ways. LAT may be taken low (HSK low) by writing a low into bit AD1 at address >0114 or when HSK is taken low by any unit on the bus and LAT was previously high. LAT can be set high by writing a high into bit AD1 at address >0114. LAT can be disabled (held high) by writing a high to the LATD bit (AD7 at address >0114). LATD is always cleared (by hardware) on a 0 to 1 transition on BAV. The status of LATD (AD7), LAT (AD1), and HSK (AD0) may be checked by reading address >0114.

SECTION 5

Keyboard (write) Latch

5.1 General Information

The processor, when writing to the B port (address >0106), will put the lower nibble of the data on the B0-B3 output lines and the upper nibble of the data on the C port (AD4-AD7). The Keyboard Latch will latch this upper nibble data and route it to the keyboard on the B4-B7 lines. This allows a full byte transfer to the keyboard while making use of the B port. The Keyboard (write) Latch is configured as shown below with bits 0-3 not being used.

7	6	5	4	3	2	1	0
B7	B6	B5	B4	X	X	X	X

When reading address >0106, B4 - B7 will be passed as data on AD4 - AD7. The B0 - B3 data is read internally by the processor.

SECTION 6

Power-on Hold Latch

6.1 General Information

One of the first steps in the power up sequence will be to write a high to the Power-on Hold Latch (POH) at bit 0 of address >0111. This will insure that the power up sequence can continue after the user has released the ON key. This also provides a means of holding power on during the turn-off sequence. The last step in the power down sequence will be to write a low to bit 0 at address >0111. The latch is represented in the figure below:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	POH

SECTION 7

Signal List

Signal Name	Function
AD0 - AD7	Data and Low Order Address
A8 - A15	High Order Address
A0 - A7	Latched Low Order Address
ALATCH	Address Latch from MLP
CLKOUT	Clock from MLP
ENABLE	Enable from MLP
R/W	Read/Write from MLP
X1, X2	Connections for Clock Crystal
CLK	Controlled Clock
Vdd, Vss	Power, Ground
B4 - B7	Keyboard (write) Data
D0 - D3	I/O Bus Data
BAV	I/O Bus Available
HSK	I/O Bus Handshake
PC1 - PC4	Page Control (Mapping)
POH	Power-on Hold

Signal Name	Function
CE1	Display Driver Chip Enable
CE2, CE3	System RAM Chip Enables
CE4, CE5	Expansion Area Chip Enables
CE6	System ROM Chip Enable

SECTION 8

Quick Reference Chart

NAME	ADDRESS	BIT ASSIGNMENTS							
		7	6	5	4	3	2	1	0
Keyboard (write)	>0106	B7	B6	B5	B4	X	X	X	X
		7	6	5	4	3	2	1	0
System Control Register	>0119	X	X	X	PC4	PC3	PC2	PC1	BCE
		7	6	5	4	3	2	1	0
Address Control Register	>0110	X	X	EAC2	EAC1	SRAC2	SRAC1	ESC2	ESC1
		7	6	5	4	3	2	1	0
Power-on Hold	>0111	X	X	X	X	X	X	X	POH

NAME	ADDRESS	BIT ASSIGNMENTS							
		7	6	5	4	3	2	1	0
I/O Bus - Data Latch	>0112	X	X	X	X	D3	D2	D1	D0
		7	6	5	4	3	2	1	0
I/O Bus - Bus Available	>0113	X	X	X	X	X	X	X	BAV
		7	6	5	4	3	2	1	0
I/O Bus - Handshake	>0114	LATD	X	X	X	X	X	LAT	HS

NOTE

All bit assignments indicated by an "X" are not available for use. Hardware latches/registers do not exist for these bits at the addresses specified.